

In the Drawings

Figure 3 Add label "SAMPLING CLOCK 70" to line between VCO/INTEGRATOR 38 and DATA RECOVERY 40;
Add line labeled "LEADING CLOCK 72" between VCO/INTEGRATOR 38 and A RECOVERY 40;
Add bus between VCO/INTEGRATOR 38 and PHASE INTERPOLATOR 44;
Add label "EARLYB" to line between DATA RECOVERY 40 and PHASE SELECT CIRCUIT/FILTER 42;
Add label "PHCODE 82" to line between PHASE SELECT CIRCUIT/FILTER 42 and PHASE INTERPOLATOR 44; and
Add line labeled and "PHMUX" between PHASE SELECT CIRCUIT/FILTER 42 and PHASE INTERPOLATOR 44.

FIG. 2
(PRIOR ART)

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graph LR
    REFCLK --> PFD
    PFD --> FILTER1[FILTER]
    FILTER1 --> VCO
    VCO --> K
    K --> PFD
    VCO --> INTCK90[INTERPOLATOR CK90]
    VCO --> INTCK0[INTERPOLATOR CK0]
    INTCK90 --> HSBUF1[HIGH SPEED CLOCK BUFFER]
    INTCK0 --> FILTER2[FILTER]
    FILTER2 --> DR[DATA RECOVERY]
    DATA --> DR
    HSBUF1 --> DR
    DR --> PFD
```

FIG. 4

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DATA OUTPUT 8

rx0 60 61 rxd0 62 63 rxd1 64 rx2 65 rxd2 66 rx3 67 rxd3

ck0 50 52 54 56 ck1 ck2 ck3 ck4 ck5 ck6 ck7

38